Amendments to the Specification

Please replace the paragraph beginning on page 16, line 16, with the following rewritten paragraph.

In addition, the etch processes of Figs. 3-5 may include forming ~~a~~ semiconductor structures 42 within semiconductor topography 20 as shown in Fig. 6. ~~-~~Semiconductor structures 42 may include, for example, gate structures or interconnect lines. In a preferred embodiment, semiconductor structures 42 may include dimension 44 within a critical dimension specification of the device. Such a critical dimension specification may be the same as used for a similar device formed from conventional etch processes. As such, the etch processes of Fig. 3-5 may not alter the critical dimension budget of the device. For example, the critical dimension of a device may be 0.17 microns +/- 20 nm using either conventional etch techniques or the method described herein. As such, dimension 44 may be between 0.16998 microns and 0.17002 microns in such an embodiment.

Please replace the paragraph beginning on page 20, line 5, with the following rewritten paragraph.

Regardless of whether resist 58 and/or anti-reflective layer 56 has been removed from semiconductor topography 50, exposed portions of semiconductor layer 52 may be removed to form trenches 64 as shown in Fig. 11. Such an etch process may be performed in the same etch chamber as the etch processes of Figs. 8 and 9. In particular, etching semiconductor layer 52 may include placing semiconductor topography 50 into an etch chamber designed to etch materials comprising silicon. Such an etch chamber may be a plasma etch tool adapted to produce a plasma density between approximately 2.0×10^{9} molecules/cm^3 and approximately 2.0×10^{11} molecules/cm^3. In addition, the etch tool may be adapted to maintain the temperature of semiconductor topography 50 between approximately 25 °C and 90 °C during the etch process of Fig. 11. Moreover, the etch chamber used for the etch processes of Figs. 3-5 may include a pressure between approximately 0.4 mTorr and approximately 50 mTorr. In an alternative embodiment, the etching of semiconductor layer 52 may be conducted in a different etch chamber than that of cap layer 54 and anti-reflective layer 56. Alternatively, semiconductor layer 26-52 may be etched in the same etch chamber as cap layer 54, but a different chamber than anti-reflective layer 56. The etch chemistry used to etch semiconductor layer 52 may include, for example, CF_3Br. In some embodiments, the etch chemistry used to etch device layer 26 may include HBr and/or NF_3.

Please replace the paragraph beginning on page 22, line 5 with the following rewritten paragraph.

Preferably, trenches 64 may be used to subsequently form shallow trench isolation regions within semiconductor layer 52. Such isolation regions may be field oxide regions, which may serve to isolate separate active regions on semiconductor layer 52 from one another. In another embodiment, trenches 64 may be used for the formation of, for example, contact structures using a ~~dual~~ Damascene process. In such an embodiment, trenches 64 may be configured to extend to a conductive region within semiconductor layer 52. The conductive region may be, for example, an underlying interconnect line or a conductive region of a device, such as source/drain regions of a transistor. Although Fig. 11 illustrates the formation of three trenches across the illustrated portion of semiconductor layer 52, any number of trenches may be formed across the substrate in accordance with design specifications of the integrated circuit. In addition, various widths and depths of the trenches may be formed in accordance with the design specifications of the integrated circuit.